Paper No. 24

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte HIROKI KURIBAYASHI
and
SHOGO MIYANABE

Appeal No. 2003-0487
Application No. 09/158,925

ON BRIEF

Before JERRY SMITH, BARRETT and NAPPI, Administrative Patent Judges.

NAPPI, Administrative Patent Judge.

DECISION ON APPEAL

This is a decision on the appeal under 35 U.S.C. § 134 from the examiner's rejection of claims 1 through 14.

The Invention

The invention relates to a clock generator for a recorded signal reading device (see appellants' specification page 3). The device contains three reading means to

read data recorded on three tracks of the recording media. The output of these readers is amplified and input into a crosstalk removing circuit (see figure 2 and page 5 of appellants' specification). The output of the crosstalk removing circuit is input to a phase detecting circuit that detects phase error. This phase error is then used to generate a clock signal (see page 9 of appellants' specification).

1. A clock generator in a recorded information reproduction apparatus for reproducing recorded information from a recording medium, comprising:

a pickup which produces a reading signal by reading a recording track of the recording medium;

a sampling circuit which samples the reading signal at a timing corresponding to a clock signal and produces a reading sample value sequence;

a crosstalk removing circuit which removes crosstalk components from the reading sample value sequence and produces a crosstalk removed reading sample value sequence, the crosstalk components being present in recording tracks adjacent to the recording track read by the pickup;

a phase detecting circuit which detects a phase error existing in the reading signal based on the crosstalk-removed reading sample value sequence; and

a clock signal generating circuit which generates the clock signal based on the phase error.

References

Hayashi	5,657,312	Aug. 12, 1997 (filed March, 13 1995)
Iwanaga (Japanese patent)	JP 3-178040	Aug. 2, 1991

Rejections at Issue

Claims 1 through 14 stand rejected under 35 U.S.C. § 103 as being unpatentable over applicants' admitted prior art of figure 1 in view of Iwanaga. Claims 1 through 14 stand rejected under 35 U.S.C. § 102 as being anticipated by Hayashi.[1]

Opinion

We have carefully considered the subject matter on appeal, the rejections advanced by the examiner and the evidence of obviousness and anticipation relied upon by the examiner as support for the rejections. We have, likewise, reviewed and taken into consideration, in reaching our decision, the appellants' arguments set forth in the briefs,[2] along with the examiner's rationale in support of the rejections and arguments in rebuttal set forth in the examiner's answer.

With full consideration being given to the subject matter on appeal, the examiner's rejections and the arguments of appellants and examiner, for the reasons stated *infra*, we reverse both the examiner's rejection of claims 1-14 under 35 U.S.C. § 103 and the examiner's rejection of claims 1-14 under 35 U.S.C. § 102.

Appellants' arguments directed to the rejection of claims 1 through 14 under 35 U.S.C. § 103 are on pages 8 through 17 of the brief. On page 14 of the brief appellants argue:

[1] The Examiner states on page 1 of the answer that the rejection based upon 35 U.S.C. § 112, second paragraph, and the rejection based upon 35 U.S.C. §103 which uses Hayashi (U.S. Patent No. 5,455,813) are withdrawn.

[2] Appellants filed an appeal brief dated June 6, 2002 and a reply brief dated January 3, 2003. The examiner mailed out an Office communication on April 9, 2003 stating that the reply brief has been considered.

> [N]either Fig. 6 nor the rest of the *Iwanaga* reference teaches or suggests a system where a phase detector (or phase detecting means) detects a phase error "based on" or "existing in" a crosstalk-removed reading sample value sequence, as required by independent claims 1, 4, 7, 10, or 13-14, respectively.

The examiner responds to this argument on page 5 of the answer stating that figure 6 of Iwanaga teaches a crosstalk extracting circuit and:

> Hence, by use of the cross talk extracting ability and provision thereof to an error extracting circuitry, the operation of this circuit parallels that of appellants' figure 4. Therefore, the examiner concludes errors (phase) either exists [sic, exist] or is [sic, are] present and modification of the acknowledged prior art figure 1 would lead to the claimed invention.

Further, on page 6 of the answer the examiner argues:

> With respect to the argument(s) presented that even if the above teachings one would still not be able to modify the primary reference in order to meet the claimed limitations, the examiner concludes that once the problem – crosstalk is recognized by the secondary reference, the positioning/placing of the appropriate element(s) to correct for such as close as possible to the source so as to mitigate against any negative impact on down stream circuits/processing is sufficient motivation to modify the primary reference and meet the claimed limitations.

We are unclear as to whether the examiner, by analogizing Iwanaga's figure 6 with appellants figure 4, is arguing that Iwanaga teaches the limitation of a phase detector, the output of which is used to generate a clock, or that the combination of the references teaches this limitation. Regardless, we do not find that Iwanaga teaches or suggests a phase determination circuit (or means) that detects a phase error in a cross talk removed signal, and that the phase error is used to generate a clock.[3]

[3] We note that the claimed phase error circuit is shown in appellants' figure 2.

Before we further discuss the teachings of the reference we must first determine the scope of the claims. We find that the scope of each of the independent claims includes a phase detector, which detects a phase error in a cross talk removed sample value sequence, and a clock signal is generated based upon this error. See the following limitations of claims 1 and 4: "a phase detecting circuit which detects a phase error existing in the reading signal based on the crosstalk removed reading sample value sequence; and a clock signal generating circuit which generates the clock signal based on the phase error." See also the following limitations of claims 7 and 10: "phase detecting means for detecting a phase error existing in the reading signal based on the crosstalk removed reading sample value sequence; and clock signal generating means for generating the clock signal based on the phase error." See the following limitations of claim 13: " a phase detecting circuit which detects a phase error existing in the crosstalk-removed reading sample value sequence; and a clock signal generating circuit which generates the clock signal based on the detected phase error." Finally, see the following limitations of claim 14 " phase detecting circuit detects a phase error existing in the crosstalk-removed reading sample value sequence and produces a detected phase error at the output of the phase detecting circuit; and a clock signal generating circuit having an input coupled to the output of the phase detecting circuit.

We do not find that Iwanaga, in figure 6 and the description of figure 6 on pages 6 though 8 of the translation, teaches that a phase determination circuit detects a phase error in a crosstalk removed sample value sequence, and that the phase error is used to generate a clock. While Iwanaga's disclosure on page 6 of the translation states that

the circuit shown in figure 6 does eliminate crosstalk, there is no disclosure that the circuit determines phase error and uses the phase error to generate a clock. Inasmuch as the examiner's statement on page 5 of the answer implies that Iwanaga's error signal detection circuit 32 is the equivalent to the phase detector, we do not find this equivalence to be proper. Iwanaga teaches, on page 7 of the translation, that the error signal detection circuit provides an output to the variable filter control circuit to adjust the frequency characteristics of filters items 26 through 28. The only discussion we find in Iwanaga's disclosure of a reading signal being used to generate a timing signal is on page 6 of the translation and this is in relation to item 23, which figure 6 shows receives a signal read from the medium before the cross talk is removed.

Further, we do not find that either the prior art or Iwanaga provides motivation to make the claimed invention. It is the burden of the examiner to establish why one having ordinary skill in the art would have been led to the claimed invention by the express teachings or suggestions found in the prior art, or by the implication contained in such teachings or suggestions. In re Sernaker 702 F.2d 989, 995, 217 USPQ 1, 6 (Fed. Cir. 1983). "Additionally, when determining obviousness, the claimed invention should be considered as a whole; there is no legally recognizable "heart' of the invention." Para-Ordnance Mfg. Inc. v. SGS Importers Int'l Inc., 73 F3d 1085, 1087, 37 USPQ2d 1237, 1239 (Fed. Cir. 1995) (citing W.L. Gore & Assocs., Inc. Garlock, Inc., 721 F.2d 1540, 1548, 220 USPQ 303, 309 (Fed. Cir. 1983), cert. denied, 469 U.S. 851 (1984)). We find that the motivation provided by the examiner to combine the references is unsupported by the evidence made of record. Appellants' admitted prior

art does not recognize the problem of crosstalk and Iwanaga does not identify an impact of crosstalk on the clock. The only teaching we find in Iwanaga that addresses the relation between the clock and crosstalk is on page 6 of the translation which identifies that the crosstalk removal circuit's effectiveness is reduced if the clock operates at the bit rate. To prevent this reduction in effectiveness, Iwanaga teaches that the clock should operate at twice the bit rate. Thus, we do not find that either of the references provides a teaching or suggestion to use a phase detector, which detects a phase error in a cross-talk removed sample value sequence, and a clock signal is generated based upon this error. Accordingly, we will not sustain the rejection of claims 1 through 14 under 35 U.S.C § 103.

We next consider the rejections of claims 1 through 14 under 35 U.S.C § 102. Appellants argue on pages 18 and 19 of the brief that Hayashi does not disclose a phase detecting circuit that detects phase errors in a crosstalk removed sample value sequence, and a clock signal is generated based upon this error. Appellants point out that Hayashi does teach in the embodiment of figure 3 a circuit that produces a cross-talk removed signal S_B. However, appellants assert that "the crosstalk-removed reading signal S_B is not used by a subsequent phase detecting circuit to detect a phase error in the reading signal in the manner required by appellants' claims" (page 19 of brief). Further, on page 20 of the brief, appellants argue that the embodiment shown in figure 9 of Hayashi "does not disclose a phase detecting circuit (or phase detecting means) which detects a phase error 'based on' or 'existing in' the 'crosstalk-removed reading sample value sequence,' as recited."

On page 7 of the answer, the examiner responds that for the rejection he is relying on figure 9, not figure 3, of Hayashi to teach the phase error detection circuit. The examiner asserts that Hayashi teaches "in column 8, lines 12-15, the sum (output of ADD element in fig. 9) is indeed a signal whose cross talk has been cancelled (removed)."

Anticipation is established only when a single prior art reference discloses, expressly or under the principles of inherency, each and every element of a claimed invention as well as disclosing structure which is capable of performing the recited functional limitations. RCA Corp. v. Applied Digital Data Systems, Inc., 730 F.2d 1440, 1444, 221 USPQ 385, 388 (Fed. Cir.); cert. dismissed, 468 U.S. 1228 (1984); W.L. Gore and Associates, Inc. v. Garlock, Inc., 721 F.2d 1540, 1554, 220 USPQ 303, 313 (Fed. Cir. 1983), cert. denied, 469 U.S. 851 (1984).

We disagree with the examiner's rejection. As stated *supra,* we find that the scope of the independent claims includes a phase detector, which detects a phase error in a "cross talk removed reading sample value sequence," and a clock signal is generated based upon this error. We find that Hayashi teaches in column 8, lines 13 to 16 that "the affection of cross talk is cancelled in the phase error signal," the output of item "ADD" in figure 9. However, we do not consider the "ADD" element to perform the same function as the claimed phase detection circuit. Hayashi does not teach that the input to the phase error signal is a crosstalk removed sample value sequence, as is required by the claims. We find that the canceling of crosstalk in Hayashi's phase error signal is due to placement of the control pits on the encoded media being read by the

device and selecting the timing of sampling at t_1 and t_2 such that there are opposite polarities (see also Hayashi, column 8, lines 10-12). Thus, Hayashi does not teach all of the limitations of claims 1 through 14. Accordingly we will not sustain the rejection of claims 1 through 14 under 35 U.S.C. § 102.

In view of the forgoing, we will not sustain the rejection of claims 1 through 14 under either 35 U.S.C. § 103 or 35 U.S.C. § 102. Therefore the decision of the examiner rejecting claims 1 through 14 is reversed.

REVERSED

JERRY SMITH Administrative Patent Judge	)	
LEE E. BARRETT Administrative Patent Judge	)	BOARD OF PATENT APPEALS AND INTERFERENCES
ROBERT E. NAPPI Administrative Patent Judge	)	

REN:clm

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